REMARKS

Claims 2-13, 15-25, and 27 were pending in the application.

Claims 2-5, 10, 11, 17, 18, 22 and 23 stand rejected under 35 U.S.C. § 102(e) as anticipated by MacPherson (U.S. Pat. No. 6,369,437). Claim 2 recites a package including at least one pair of programmable elements, the one pair including the one one-time programmable element and a second one-time programmable element, the second one-time programmable element having a first and second end, the first end of the second one-time programmable element coupled to a second power supply voltage node and the second end of the second one-time programmable element being coupled through an internal package node to the second end of the first -one-time programmable element.

The structure claimed by claim 2 (subject matter originally in claim 14) is illustrated in Figs. 6-10 of the application, where pairs of programmable elements, e.g., elements 601 and 602 are shown. Note that in the embodiment illustrated in Figs. 6-10, at least one fuse of each pair must be blown to connect the common node to either of the supply voltages Vcc or Vss. Note that if three state logic is available, then both fuses of the pair can be cut to represent a third value. Applicants respectfully submit that the structure in amended claim 2 and illustrated in Figs. 6-10 is not shown in MacPherson. The Office Action states that MacPherson discloses fuses formed for an integrated circuit die. Claim 2 specifically recites a package including at least one pair of programmable elements. MacPherson fails to teach a package having a pair of programmable elements. Accordingly, applicants respectfully submit that claim 2 and therefore claims 3-5, 10, 11, which depend on claim 2, are patentably distinguishable over MacPherson.

Similarly, claim 17 recites a package including one or more one-time programmable elements. MacPherson fails to teach a package having one-time programmable elements. Accordingly, applicants submit that claim 17 distinguishes over MacPherson. Claims 18, 22 and 23, which depend from claim 17, distinguish over MacPherson for at least the reason given for claim 17.

Claims 2, 7-9, 11, 12, 15-18, 20-23 and 27 stand rejected under 35 U.S.C. §102(b) as being anticipated by Crafts (U.S. Pat. No. 5,536,968). Crafts teaches a programmable read only

memory (PROM) including an array of polysilicon fuse elements. See Abstract. Crafts fails to teach anything about one-time programmable elements being located on a package for mounting a semiconductor die as required by independent claims 2, 12, 17, and 21. The fact that memory devices are conventionally placed in dies in semiconductor packages fails to teach one-time programmable elements, such as fuses, on the package (not in a die which is mounted in the package). Accordingly, applicants respectfully submit that the independent claims distinguish over Crafts and respectfully request that the rejection of those claims and all claims dependent thereon be reconsidered and withdrawn.

Claim 12 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Hamdy (U.S. Pat. No. 5,266,829). Amended claim 12 recites that another programmable element is serially coupled between the second end of the programmable element and an external package connection. That structure is shown, for example, in Fig. 8 where programmable elements 624-627 are coupled between the second end of programmable element 601-607 and external package connectors. The structure illustrated in Fig. 8 provides, as described on page 10, lines 3-7 of the application, that the fuses 624-627 can be used in testing environments, where, for example, an internal signal must be accessible during test, but is then decoupled from the package pin by blowing a fuse prior to product shipment. That claimed structure and the advantage referenced above is not taught or suggested in any of the references of record alone or in combination. Hamdy is directed towards electrically programmable interconnect devices for use in integrated circuits. Hamdy fails to teach anything related to one time programmable elements on packages. Further, the Office Action points to elements 168d in Fig. 5a of Hamdy and asserts that element 168h is coupled between a second end of antifuse 168d and output 178. According to the Office Action, the first end of antifuse 168d is coupled to bit line 00 (the power supply). The applicants note that the second end of antifuse 168d is coupled either to ground through transistor 166d or is floating if the antifuse is not programmed. Thus, the element 168h cannot be coupled between the second end as required by the claim and an external package connection.

If view of the above amendments and remarks applicants submit that claim 12 is in condition for allowance.

Claims 13 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Nathan (U.S. Pat. No. 5,813,881). Claim 13 has been canceled rendering the rejection moot.

Claim 21 stands rejected under 35 U.S.C. §102(b) as being anticipated by Best (U.S. Pat. No. 5,748,031). Best teaches fuses in integrated circuit and fails to teach, as required by claim 21, a package containing one or more one-time programmable elements and an integrated circuit die mounted in the package. Accordingly, applicants submit that claim 21 distinguishes over Best.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over MacPherson. Applicants submit that claim 6 distinguishes over MacPherson at least for the reasons given for claim 2.

Claims 19, 24, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Macpherson further in view of Barth (U.S. Pat. No. 5,134,616). As applicants explained, MacPherson fails to teach a package including one or more one-time programmable elements as recited in claim 17, on which claims 19 and 24 depend and in claim 25. That teaching is not supplied in Barth. Accordingly, applicants respectfully request that the rejection of claim 19, 24, and 25 be reconsidered and withdrawn. Further, Barth fails to teach, as recited in claim 19 that the one or more one-time programmable elements specify an operating voltage of at least a portion of a processor. Thus, applicants respectfully request that the rejection of claim 19 be reconsidered and withdrawn for that additional reason.

Barth and MacPherson, alone or in combination also fail to teach, as recited in claim 24, that the one or more one-time programmable elements specify a control value relating to clock frequency at which the processor operates. Thus, applicants respectfully request that the rejection of claim 19 be reconsidered and withdrawn for that additional reason.

The Office action rejects claim 25 relying on MacPherson and Barth, col. 12, lines 10-34, to teach a semiconductor memory device wherein fuses are programmed to perform an error correction. However, that fails to teach that the claimed programmable element specifies use of ECC for the cache memory on the integrated circuit as claimed in claim 25. Instead Barth teaches using fuses to achieve redundancy by efficiently switching in redundant bit lines. See

Summary of the Invention. Barth fails to teach or suggest specifying use of ECC using a programmable element as claimed in claim 25. Accordingly, applicants respectfully submit that claim 25 distinguishes over the references of record.

In view of the above amendments and remarks, applicants believe that all claims are now in condition for allowance. However, if the Examiner believes there are any issues which could be resolved via a telephone conference, the Examiner is respectfully requested to contact the undersigned at the number indicated below.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

Mark Zagorin 10/3/02
Mark Zagorin Date

Respectfully submitted,

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MARKED-UP COPY OF AMENDED CLAIMS IN ACCORDANCE WITH 37 C.F.R. § 121(c)(ii)

12. (Twice Amended) A package for mounting at least one integrated circuit die, the package comprising at least one one-time programmable element having a first and a second end separated by a programmable link, wherein the first end of the one-time programmable element is coupled to a power supply voltage node in the package and wherein the package further comprises another programmable element serially coupled between the second end of the programmable element and an external package connection.